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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/476,678	12/30/1999	PHILIP NORD JENKINS	499.028US1	8138

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EXAMINER	
MUNOZ, GUILLERMO	

ART UNIT	PAPER NUMBER
2634	19

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/476,678	JENKINS ET AL.	
	Examiner	Art Unit	
	Guillermo Munoz	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed March 12, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-39 and 42-44* is/are allowed.

6)☒ Claim(s) *1,2,10,40 and 41* is/are rejected.

7)☒ Claim(s) *3-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see amendment, filed March 12, 2004, with respect to claims 25-26 have been fully considered and are persuasive. The rejection of claims 25-26 has been withdrawn.

Withdrawal of Allowability

The indicated allowability of claims 1-10 and 40-41 is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg et al. in view of Feraiolo et al.

Regarding Claim 1

Examiner's Broadest Interpretation of Claim 1:

The difference of arrival time between the transmitted clock and plurality of signals is detected. The method of detection is not specified and is interpreted to be any method generally available to the public at the time of the invention. Delay is added to the received signals to compensate the detected difference of arrival time of each signal with

the transmitted clock. The phase of the plurality of received signals is compared to a reference signal to detect changes in the detected difference of arrival time. The reference signal is interpreted as being either the received transmitted clock signal or a regenerated version of the transmitted clock signal, since, according to applicants argument in amendment filed May 29, 2003, the phase comparison does not involve pattern matching. The delay added to the received signals is modified to adapt to changes in the detected difference of arrival time between the transmitted clock and plurality of signals.

Prior Art:

Gregg et al. disclose all the subject matter claimed as follows: data is transmitted along separate conducting lines along with a transmit clock signal that is transmitted on a separate line, note Col. 1, lines 60-62. At the receiver, the data on each line is separately phase aligned with the clock, note Col. 1, lines 62-64. The phase alignment has an inherent requirement of detecting the phase difference between the data on each line with the clock. Gregg et al. suggest that the bit phase alignment is performed at the self-timer (element 52 of figure 3). However, Gregg et al. leaves the discloser of the operation of the self time to patents incorporated by reference, note Col. 1, lines 7-32 and Col. 3, lines 47-49.

Ferraiolo et al. disclose a self-time interface, which teach three incrementally selectable delay elements used with data edge detection circuitry to successfully detect a data early phase, data late phase, and data on-time phase. The edge detectors generate a "lead", "lag", or "do nothing" control signal used to shift the phase of the data coupled to

RES-FES latches. Ferraiolo et al. teach an initialization process wherein bulk delays are reset to their minimum delay and during normal operations the small updates will be made to track temperature, power supply, and data jitter by adding delay in the fine delay elements section.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to define Gregg et al.'s self timer with Ferraiolo et al.'s disclosure of using adjustable delay lines for each of the received data signals for the purpose of aligning each of the received signals with the received clock signal, since Gregg et al. suggest such a combination in Col. 1, lines 7-32.

Regarding Claim 2

Examiner's Broadest Interpretation of Claim 2:

The phrase "generating a clock early signal and a data early signal" is interpreted as meaning generating a clock early signal if the clock phase leads the data phase or generating a data early signal if the data phase leads the clock phase.

Prior Art

As applied to claim 1, Ferraiolo et al. do not explicitly teach the claimed subject matter, however, the functionality of the "lead", "lag", or "do nothing" signal is the same, see Col. 5, lines 25-27.

Regarding Claim 10

Gregg et al. further teach the claimed subject matter in figure 3, element 62.

Claims 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg et al. in view of Jordan et al.

Examiner's Broadest Interpretation of Claim 40:

The phrase "driving the circuitry with a predefined sequence of data edges" is broadly interpreted as receiving as input a data signal that has a predefined sequence of data edges. The phrase "driving the phase comparator with a clock" is broadly interpreted as supplying the phase comparator with a clock for the purpose of comparing the clock phase with the received data signal phase. The phrase "indicating drift from the 50% duty cycle" is broadly interpreted as indicating a drift of the data bit from the sample point of the clock edge, that is, the drift indicates a phase error between the received data signal and a clock signal.

Prior Art:

Gregg et al. disclose all the subject matter claimed as follows: data is transmitted along separate conducting lines along with a transmit clock signal that is transmitted on a separate line, note Col. 1, lines 60-62. At the receiver, the data on each line is separately phase aligned with the clock, note Col. 1, lines 62-64. The phase alignment has an inherent requirement of detecting the phase difference between the data on each line with the clock. Gregg et al. suggest that the bit phase alignment is performed at the self-timer (element 52 of figure 3). However, Gregg et al. leaves the discloser of the operation of the self time circuitry to patents incorporated by reference, note Col. 1, lines 7-32 and Col. 3, lines 47-49.

Jordan et al. teach an edge detection circuit used in a phase locked loop wherein a received data signal is phase compared with a clock signal. The alignment process is repeated until the data edges are aligned with the positive going edge of the clock. The clock frequency is twice the data frequency, thereby allowing the center of the data bit to be sampled by the falling edge of the clock, note Col. 2, lines 4-24. A clock signal characterized as having positive edges aligned to the edges of a data bit and falling edges at midpoint between data edges can be further characterized as having a 50% duty cycle.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to define Gregg et al.'s self timer with Jordan et al.'s disclosure of using a clock with twice the frequency for each of the received data signals for the purpose of sampling each of the received signals at midpoint, since Gregg et al. suggest such a combination in Col. 1, lines 7-32.

Claims 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gregg et al. in view of Jordan et al. and Ferraiolo et al.

As applied to claim 40 above, Gregg et al's self time circuitry incorporates the discloser of Ferraiolo et al., note Col. 1, lines 7-32 and Col. 3, lines 47-49.

Ferraiolo et al. teach the claimed subject matter in figure 5, elements 80 and 82.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to define Gregg et al.'s self timer with Ferraiolo et al.'s disclosure of using a coarse delay line, since Gregg et al. suggest such a combination in Col. 1, lines 7-32.

Claim Objections

Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

Claims 11-39, and 42-44 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 11-24, 27-39, and 43-44 are considered allowable because the present invention comprises a detection of skew between the received transmit clock and each of a plurality of received data signals and a controller used to modify delay of the received data signals based on the detected skew. The closest prior art, Gregg et al., (US Patent Number 5,598,442) shows a similar circuit including a detection of skew between a plurality of received data signals. However, Gregg et al fails to teach a single controller for modifying delay of the received data signals based on the detected skew. This distinct feature of the instant application has been included in independent claims 11, 27, and 39 rendering them allowable.

Claims 25-26 are considered allowable because the present invention comprises a delay line controller for controlling a plurality of delay lines. The controller has a plurality of skew indicator signal inputs, each input having a digital filter connected to it that generates a delay control signal. The closest prior art, Sakamoto et al. (cited in previous office action) shows a similar circuit including a controller for controlling the delay of a plurality of delay lines. However, Sakamoto et al. fails to teach each skew signal input having a digital filter for

generating a delay control signal. This distinct feature of the instant application has been included in independent claim 25 rendering it allowable.

Claim 44 is considered allowable because the present invention comprises a method for adaptively deskewing delays between a plurality of channel signals comprising the steps of determining a data minus clock value for each received channel signal; varying the value depending on the skew of the received channel signal and a reference signal; determining a minimum value; setting a delay of the received clock based on the minimum value; and calculating a channel signal delay based on the difference between the minimum value and the value of each channel signal. None of the references of record teach the limitations. These distinct features of the instant application have been included in independent claim 42 rendering it allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 703-305-4224. The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guillermo Muniz

GM
May 20, 2004

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